Listing of Claims

1. (Currently amended) A delay-locked-line (DLL) comprising:

a voltage-controlled delay line (VCDL) that varies a timing of the delayed clock signal with respect to an intermediate clock signal in response to a magnitude of a control voltage;

a phase detector connected to the VCDL that detects a difference in phase between a reference clock signal and the delayed clock signal, the phase detector asserting an up signal when the reference clock signal leads the delayed clock signal, a down signal when the reference clock signal lags the delayed clock signal, and a synch signal when the reference clock signal and the delayed clock signal are in phase;

a charge pump connected to the phase detector that outputs a pump voltage, the charge pump increasing the pump voltage when the up signal is asserted, decreasing the pump voltage when the down signal is asserted, and leaving the pump voltage unchanged when the synch signal is asserted;

a filter connected to the charge pump and the VCDL that filters the pump voltage to output the control voltage; and

a delay circuit that varies a timing of the intermediate clock signal with respect to the reference clock signal by adding or subtracting incremental units of delay in response to the control voltage and the logic states of the up signal, the down signal, and the synch signal[[.]], and

wherein the VCDL includes:

a voltage-controlled current stage that outputs a switching current having a magnitude defined by the magnitude of the control voltage; and

a fine-delay stage having a number of devices, the devices having a propagation delay, a magnitude of the propagation delay being defined by the magnitude of the switching current, the delayed clock signal being delayed in time from the intermediate clock signal by the propagation delay.

2. (Cancelled)

3. (Currently amended) The DLL of claim [[2]] 1 wherein the phase detector includes:

a D-Q flip-flop having a D input connected to receive the delayed clock signal, a clock input connected to receive the reference clock signal, and a Q output;

an XNOR gate having a first input connected to receive the delayed clock signal, a second input connected to receive the reference clock signal, and an output;

a first inverter having an input connected to the Q output, and an output;

a second inverter having an input connected to the output of the first inverter, and an output;

a first NOR gate having a first input connected to the output of the XNOR gate, a second input connected to the output of the second inverter, and an output that outputs the up signal; and

a second NOR gate having a first input connected to the output of the XNOR gate, a second input connected to the output of the first inverter, and an output that outputs the down signal.

4. (Currently amended) The DLL of claim [[3]] 2 wherein the phase detector further includes:

a first rising edge detecting circuit that receives the reference clock signal, and asserts a reference pulse having a predefined width in response to the rising edge of the reference clock signal;

a second rising edge detecting circuit that receives the delayed clock signal, and asserts a delayed pulse having a predefined width in response to the rising edge of the reference clock signal; and

a logic circuit that outputs the synch signal when the reference pulse and delayed pulse are asserted and overlap.

5. (Original) The DLL of claim 1 wherein the phase detector includes:

a first rising edge detecting circuit that receives the reference clock signal, and asserts a reference pulse having a predefined width in response to the rising edge of the reference clock signal;

a second rising edge detecting circuit that receives the delayed clock signal, and asserts a delayed pulse having a predefined width in response to the rising edge of the reference clock signal; and

a logic circuit that outputs the synch signal when the reference pulse and delayed pulse are asserted and overlap.

6. (Original) The DLL of claim 1 wherein the delay circuit includes a number of delay blocks, each delay block having a first predetermined delay when turned on, and a second predetermined delay when turned off, the second predetermined delay being less than the first predetermined delay.

7. (Original) The DLL of claim 1 wherein the delay circuit includes a number of delay blocks, each delay block having a first predetermined delay when inserted into a reference clock signal path, and a second predetermined delay when removed from the reference clock signal path, the second predetermined delay being less than the first predetermined delay.

8. (Original) The DLL of claim 6 wherein delay circuit further includes a control circuit that defines the amount of delay provided by the delay circuit by controlling the on-off state of the delay blocks in response to the logic states of the up signal, the down signal, and the synch signal.

9. (Original) The DLL of claim 7 wherein delay circuit further includes a control circuit that defines the amount of delay provided by the delay circuit by controlling the on-off state of the delay blocks in response to the logic states of the up signal, the down signal, and the synch signal.

10. (Original) The DLL of claim 8 wherein the control circuit includes:

a shift register having a chain of registers, the shift register shifting a logic high in a first direction of the chain each time a shift left signal is asserted, and shifting a logic low in a second direction of the chain each time a shift right signal is asserted, each register having an output connected to a corresponding delay block;

an up stage that asserts the shift right signal each time the up signal is asserted when the control voltage is in an upper range; and

a down stage that asserts the shift left signal each time the down signal is asserted when the control voltage is in a lower range.

11. (Original) The DLL of claim 10 wherein neither the shift right signal nor the shift left signal is asserted when the synch signal is asserted.

12. (Original) The DLL of claim 9 wherein the control circuit includes:

a shift register having a chain of registers, the shift register shifting a logic high in a first direction of the chain each time a shift left signal is asserted, and shifting a logic low in a second direction of the chain each time a shift right signal is asserted, each register having an output connected to a corresponding delay block;

an up stage that asserts the shift right signal each time the up signal is asserted when the control voltage is in an upper range; and

a down stage that asserts the shift left signal each time the down signal is asserted when the control voltage is in a lower range.

13. (Original) The DLL of claim 12 wherein neither the shift right signal nor the shift left signal is asserted when the synch signal is asserted.

14. (Currently amended) A method of locking a delayed clock signal to a reference clock signal, the delayed clock signal having a delay with respect to the reference clock signal, the method comprising the steps of:

varying a timing of the delayed clock signal with respect to an intermediate clock signal with a voltage-controlled delay line (VCDL) in response to a magnitude of a control voltage;

detecting with a phase detector a difference in phase between a reference clock signal and the delayed clock signal;

asserting with the phase detector an up signal when the reference clock signal leads the delayed clock signal, a down signal when the reference clock signal lags the delayed clock

signal, and a synch signal when the reference clock signal and the delayed clock signal are in phase;

outputting with a charge pump a pump voltage, the pump voltage increasing when the up signal is asserted, decreasing when the down signal is asserted, and being unchanged when the synch signal is asserted;

filtering with a filter the pump voltage to output the control voltage; and

varying a timing of the intermediate clock signal with respect to the reference clock signal with a delay circuit by adding or subtracting incremental units of delay in response to the control voltage and the logic states of the up signal, the down signal, and the synch signal[.], and

wherein the step of varying a timing of the delayed clock signal includes:

outputting a switching current having a magnitude defined by the magnitude of the control voltage; and

delaying the delayed clock signal with respect to the intermediate clock signal an amount defined by the magnitude of the switching current.

15. (Cancelled)

16. (Original) The method of claim 14 wherein the delay circuit includes a number of delay blocks, each delay block having a first predetermined delay when turned on, and a second predetermined delay when turned off, the second predetermined delay being les than the first predetermined delay.

17. (Original) The method of claim 16 and further comprising the step of defining the amount of delay provided by the delay circuit by controlling the on-off state of the delay blocks with a shift register in response to the logic states of the up signal, the down signal, and the synch signal.

18. (Original) The method of claim 17 wherein the shift register has a chain of registers, and

further including the steps of shifting a logic high in a first direction of the chain each time a shift left signal is asserted, and shifting a logic low in a second direction of the chain each

time a shift right signal is asserted, each register having an output connected to a corresponding delay block;

asserting the shift right signal each time the up signal is asserted when the control voltage is in an upper range; and

asserting the shift left signal each time the down signal is asserted when the control voltage is in a lower range.

19. (Original) The method of claim 18 wherein neither the shift right signal nor the shift left signal is asserted when the synch signal is asserted.

20. (Original) The DLL of claim 1 and further comprising a reset circuit that resets each register to a logic low when the output of each register is a logic high and the shift left signal is asserted, and sets each register to a logic high when the output of each register is a logic low and the shift right signal is asserted.